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(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(72) Inventors: WOO, Christy, Mei-Chu; 10706 Linda Vista Drive, Cupertino, CA 95014 (US). WANG, Pin-Chin, Connie; 461 Burgess Drive #2, Menlo Park, CA 94025 (US).

(74) Agent: RODDY, Richard, J.; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

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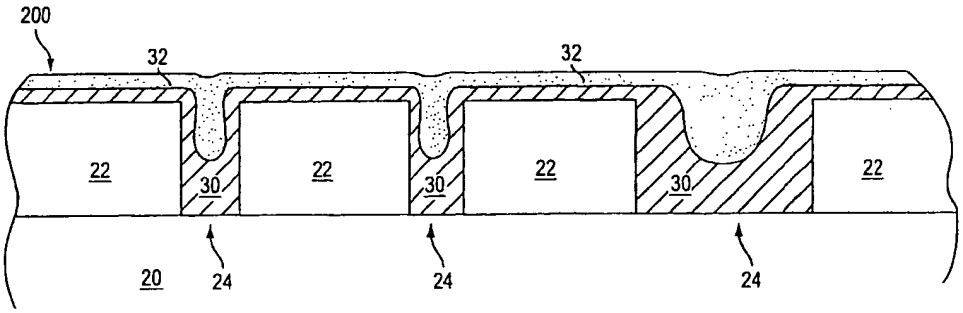
(54) Title: COPPER INTERCONNECTS WITH IMPROVED ELECTROMIGRATION RESISTANCE AND LOW RESISTIVITY



(57) Abstract: Copper interconnects are formed by depositing substantially pure copper (30) into the lower portion of an interconnect opening (24). The upper portion of the interconnect opening (24) is then filled with doped copper (32) followed by a planarization process. The resulting copper interconnect exhibits reduced electromigration while maintaining low overall resistivity.

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COPPER INTERCONNECTS WITH IMPROVED ELECTROMIGRATION RESISTANCE AND LOW RESISTIVITY

TECHNICAL FIELD

The present invention relates to a semiconductor device and a method of manufacturing a semiconductor device having copper interconnects. The present invention has particular applicability to high density semiconductor devices with submicron design features.

BACKGROUND ART

The escalating requirements for high density and performance associated with ultra large scale integration semiconductor devices require design features of 0.25 microns and under, increased transistor and circuit speeds, high reliability and increased manufacturing throughput. The reduction of design features to 0.25 microns and under challenges the limitations of conventional methodology.

Conventional semiconductor devices typically comprise a semiconductor substrate, normally made of monocrystalline silicon, and multiple dielectric and conductive layers formed thereon. In a conventional semiconductor device 100 illustrated in Fig. 1, substrate 1 is provided with field oxide 2 for isolating an active region including source/drain regions 3, and a gate electrode 4, typically of doped polysilicon, above the semiconductor substrate with gate oxide 5 therebetween. Interlayer dielectric layer 6, typically silicon dioxide, is then deposited thereover and openings formed using conventional photolithographic and etching techniques. The openings are filled with conductive material to establish electrical contact between subsequently deposited conductive layer 8 and source/drain regions 3 through contacts 7, and to transistor gate electrode 49. Dielectric layer 9, typically silicon dioxide, is deposited on conductive layer 8, and another conductive layer 10, typically aluminum or an aluminum-base alloy, is formed on dielectric layer 9 and electrically connected to conductive layer 8 through vias 11.

With continued reference to Fig. 1, conductive layer 10 is the uppermost conductive layer and, hence, constitutes the wire bonding layer. Dielectric layer 12, also typically silicon dioxide, is deposited, and a protective dielectric scratch resistant topside layer 13 is deposited thereon. Protective dielectric layer 13 typically includes a nitride layer, such as silicon nitride (Si_3N_4). Alternatively, protective dielectric layer 13 may include a dual topcoat comprising a nitride layer on an oxide layer. The protective dielectric layer 13 provides scratch protection to the semiconductor device 100 and protection against moisture and impurity contamination during subsequent processing. After deposition of protective dielectric layer 13, conventional photolithographic etching techniques are employed to form an opening to expose wire bonding layer 10 for external connection via bonding pad 14 and electrically conductive wires 15 or an external connection electrode (not shown).

Although only two conductive layers 8 and 10 are depicted in Fig. 1 for illustrative convenience, conventional semiconductor devices may include more than two conductive layers, e.g., five conductive metal layers, depending on design requirements. Also in the interest of illustrative convenience, Fig.1 does not illustrate any particular type of plug or barrier layer technology. However, such technology is conventional and, therefore, the details of such features are not set forth herein.

As device features continue to shrink in size, the interconnect structures, such as contacts 7 and vias 11 enable the semiconductor device 100 to offer more packing density, higher speeds and more flexibility in circuit design. Various metals, such as aluminum and aluminum-base alloys, have typically been used to form the electrical interconnects. More recently, copper and copper-base alloys have also been used to fill the openings to form the electrical interconnects. In such cases, the copper is typically deposited via a single electroplating process. That is, a

single plating solution employing one type of plating chemistry is supplied to an electroplating chamber where the electroplating proceeds to fill the openings that form the interconnects. One problem with copper interconnects is that copper has low electromigration resistance and readily diffuses through silicon dioxide, the typical dielectric interlayer used in the manufacture of semiconductor devices.

In some prior processes, a dopant has been added to the copper to enhance the low electromigration resistance of copper. The dopant element forms intermetallic compounds with the copper and increases the electromigration resistance of the copper. In processes that employ copper alloys, however, the copper alloy is typically deposited throughout the entire opening that will form the interconnect or deposited and annealed to diffuse the dopant element throughout the entire interconnect structure. This use of copper alloys may help solve electromigration problems, but including the dopant throughout the entire interconnect increases the resistivity of the interconnect. This increased resistivity leads to slower processing associated with the semiconductor device.

DISCLOSURE OF THE INVENTION

There exists a need for a semiconductor device and a method for manufacturing a semiconductor device that improves electromigration problems associated with copper interconnects while maintaining low resistivity of the interconnect.

These and other needs are met by the present invention, where substantially pure copper is introduced into the lower portion of an interconnect opening followed by the introduction of doped copper at the top portion of the opening. The copper interconnect is then planarized, resulting in a copper interconnect having reduced electromigration and low overall resistivity.

Additional advantages and other features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from the practice of the invention. The advantages and features of the invention may be realized and obtained as particularly pointed out in the appended claims.

According to the present invention, the foregoing and other advantages are achieved in part by a method of forming an interconnect in a semiconductor device. The method includes forming an opening in a dielectric layer and depositing substantially pure copper to fill a portion of the opening. The method also includes depositing doped copper over the substantially pure copper to fill the opening and planarizing the semiconductor device so that the filled opening is substantially coplanar with an upper surface of the dielectric layer.

According to another aspect of the invention, a semiconductor device is provided. The semiconductor device comprises a semiconductor substrate and a plurality of levels of dielectric layers and conductive layers formed on the semiconductor substrate. The semiconductor device also includes an interconnect formed in at least one of the dielectric layers. The interconnect electrically connects at least two of the conductive layers or one of the conductive layers and an active region in the semiconductor substrate. The interconnect includes a lower portion comprising substantially pure copper and an upper portion comprising doped copper.

Other advantages and features of the present invention will become readily apparent to those skilled in this art from the following detailed description. The embodiments shown and described provide illustration of the best mode contemplated for carrying out the invention. The invention is capable of modifications in various obvious respects, all without departing from the invention. Accordingly, the drawings are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference is made to the attached drawings, wherein elements having the same reference number designation represent like elements throughout.

Fig. 1 schematically illustrates the cross-section of a conventional semiconductor device.

Fig. 2A schematically illustrates the formation of interconnect openings in a dielectric layer in accordance with an embodiment of the present invention.

Fig. 2B schematically illustrates the partial filling of the interconnect openings in Fig. 2A in accordance with an embodiment of the present invention.

Fig. 3 illustrates filling the remainder of the interconnect openings in Fig. 2B, in accordance with an embodiment of the present invention.

Fig. 4 illustrates the cross-section of the semiconductor device of Fig. 3 after planarization, in accordance with an embodiment of the present invention.

Fig. 5 illustrates the cross-section of an interconnect formed in accordance with an embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention addresses and solves the problems of electromigration associated with copper interconnects while maintaining low overall resistivity of the interconnects.

Fig. 2A illustrates the cross-section of a semiconductor device 200 formed in accordance with an embodiment of the present invention. Referring to Fig. 2A, a dielectric layer 22, such as silicon dioxide or another material having a low dielectric constant (K), is formed above semiconductor substrate 20, typically comprising monocrystalline silicon. The dielectric layer 22 may also be formed of several films. For example, the dielectric layer 22 may be a composite including a low K material, a nitride layer formed thereon to serve as an anti-reflective coating (ARC) for subsequent lithographic and etching steps and a TEOS or nitride capping layer to protect the low K material. The dielectric layer 22 is shown directly above the substrate 20. It should be understood, however, that dielectric layer 22 may be an interlayer dielectric layer formed a number of layers above the surface of semiconductor substrate 20. For example, dielectric layer 22 may be an interlayer dielectric formed above a number of conductive and other dielectric layers (not shown) in semiconductor device 200.

Openings 24 are formed in dielectric layer 22 using conventional photolithographic and etching techniques. These openings 24 may represent holes for forming contacts or vias or trenches for forming interconnect lines. In Fig. 2A, three openings 24 are shown for simplicity and to illustrate various sized openings having different aspect ratios. The present invention, however, may be used to form any number of interconnects having any particular feature sizes and aspect ratios, based on the particular circuit requirements.

As discussed previously, conventional practices for forming interconnects use aluminum, aluminum-base alloys, copper or copper-base alloys. The present invention departs from conventional practices by depositing copper and a copper-base alloy in two plating processes to form the interconnect structure. Fig. 2B illustrates an exemplary embodiment of the present invention in which the first plating deposits essentially pure copper into the openings 24 using a non-conformal electroplating chemistry.

For example, the first plating process may use a plating solution that includes additives that enhance bottom filling of openings 24. Any conventional additive chemistry that is designed to enhance bottom filling, such as Nanoplate 2001 or Ultrafill 2001, both manufactured by Shipley Company of Marlborough, Massachusetts, may be mixed with the plating solution used in the first plating process. Other plating chemistries designed to enhance the filling of the bottom portion of openings may also be used.

The bottom-enhanced filling chemistry is prepared in a conventional plating solution tank and supplied to a conventional electroplating chamber to begin the first plating process. Power is supplied to the electroplating chamber where the semiconductor device 200 acts as one of the two electrodes. The electroplating proceeds to deposit the essentially pure copper into openings 24. The electroplating is monitored so that a predetermined amount of copper is deposited into the openings 24. According to an exemplary embodiment of the present invention, a layer of essentially pure copper 30 is deposited on semiconductor device 200 until the openings are about 40% to about 90% filled. For example, Fig. 2B shows the openings 24 being about 70% filled. The particular percentage that the essentially pure copper 30 fills the openings 24 may be optimized based on the particular circuit requirements, as described in more detail below. After the predetermined amount of pure copper 30 has been deposited, the first plating process is terminated.

The present invention further departs from methodology that deposits doped copper over pure copper by using a second plating process to deposit a copper alloy. According to an exemplary embodiment of the present invention, a second plating solution employing a conformal filling chemistry is prepared in a plating solution tank to fill the remaining portion of the openings 24. The second plating solution also contains a dopant to form a copper alloy in the unfilled portions of the openings 24. The dopant element used to form the copper alloy may include tin, zirconium, strontium, palladium, magnesium, chromium or tantalum. Alternatively, any other dopant element that is known to increase the electromigration resistance of copper may be used. According to an exemplary embodiment, the plating solution is designed so that the percentage weight of the dopant element in the copper alloy ranges from about 0.3% to about 12.0%, based on the particular dopant element and the particular circuit requirements, as described in more detail below. Other percentages of the dopant element may be used in alternate embodiments of the present invention.

The second plating solution is then supplied to the electroplating chamber to deposit the doped copper into the unfilled portions of the openings 24. According to an exemplary embodiment, the second plating process may be an electroless plating process. In this case, no electrical potential needs to be applied to the semiconductor device 200 while the plating process occurs. The electroless plating process relies on the autocatalytic deposition of the doped copper by the interaction of the agents in the plating solution. Alternatively, the second plating process may be an electroplating process. In either case, the second plating process deposits a layer of doped copper 32 on the semiconductor device 200 until the openings 24 are completely filled, as illustrated in Fig. 3. The layer of doped copper 32 also forms over the dielectric layer 22.

According to an exemplary embodiment of the present invention, the same plating chamber may be used for both platings, i.e., the copper plating and the copper alloy plating. In this scenario, the plating solution from the first plating is drained or returned to a holding tank and the second plating solution is supplied to the plating chamber. The supply of the two plating solutions may slightly overlap to preserve continuity and keep the surface of semiconductor device 200 from drying or starving for plating solution. Alternatively, a separate plating chamber may be used for the second plating process. In this scenario, the semiconductor device 200 is transported from the first plating chamber to a second plating chamber. Using separate plating chambers enables the first plating chamber to reuse existing plating solution used in the first electroplating process and also enables the second plating chamber to reuse plating solution used in the second plating process.

After the doped copper layer 32 has been deposited, the semiconductor device 200 is subjected to a chemical mechanical polishing (CMP) process. The CMP removes excess copper alloy 32 over the dielectric layer 22 and the filled openings 24 and planarizes the copper deposited in openings 24 with the upper surface of the dielectric layer 22.

Fig. 4 illustrates the results of the CMP of semiconductor device 200. After CMP, the pure copper 30 remains in the bottom portion of the openings 24 and the copper alloy 32 remains in the upper portion of the openings 24. Additionally, the upper surface of the filled interconnect openings 24 are substantially coplanar with the upper surface

of the dielectric layer 22. In this manner, subsequent processing steps may be performed over a substantially planar and smooth surface.

The resulting interconnect structures illustrated in Fig. 4 advantageously include the copper alloy in the areas requiring reduced electromigration, such as the upper surface of the interconnects. Additionally, the essentially pure copper is located throughout the remainder of the interconnect structure, resulting in low overall resistivity and higher speed interconnects. The particular percentage of the interconnect filled with copper versus the copper alloy may be optimized to provide increase electromigration benefits and maintain low overall resistivity. For example, in situations where operating speed is more important than increased electromigration resistance, the percentage of the interconnects that include the copper alloy may be reduced. Additionally, in such situations, the percentage of the dopant element in the copper alloy may also be reduced to further decrease the overall resistivity. In this manner, the preferential deposition of copper and a copper alloy may be optimized to provide improved electromigration while maintaining low overall resistivity.

It should be understood that Fig. 4 does not illustrate any diffusion barrier layer that may be deposited in openings 24 prior to deposition of the copper layer 30. Such diffusion barrier layers are well known and further impede the electromigration of copper into various dielectric layers. It should also be noted that Fig. 4 does not illustrate a copper alloy seed layer that may be deposited on a diffusion barrier layer to enhance the adhesion of the undoped copper layer 30 during electroplating.

According to an exemplary embodiment of the present invention, a copper alloy seed layer may be deposited along the bottom and sidewall portions of the interconnect openings 24 to carry electrical current for electroplating. In depositing a relatively thin seed layer in the interconnect openings, any number of techniques may be used.

For example, Fig. 5 illustrates a copper alloy seed layer 50 conformally deposited along the sidewalls 40 and bottom 42 of the respective interconnect openings 24 in semiconductor device 300. The copper alloy seed layer 50 may be deposited using any conventional process, such as chemical vapor deposition (CVD), ionized metal plasma (IMP) deposition, physical vapor deposition (PVD) or other known processes to conformally deposit a relatively thin layer in the interconnect openings 24. The thickness of the copper alloy seed layer 50 may range from about 200 Å to about 1000 Å, depending on the particular circuit requirements.

The dopant element in the copper alloy seed layer 50 may include magnesium, aluminum, zinc, zirconium, tin, nickel, palladium, silver or gold. Alternatively, other dopant elements may be used in copper alloy seed layer 50. The percentage by weight of the dopant element in the copper alloy seed layer 50 may be optimized based on the particular device requirements. For example, the percentage by weight of the dopant element in copper alloy seed layer 50 may range from about 0.3% to about 12%, based on the particular dopant and the particular circuit requirements.

After the copper alloy layer 50 is deposited, the first and second plating processes described with regard to Figs. 2B and 3 are performed to deposit the essentially pure copper layer 30 and the doped copper layer 32. A CMP follows to planarize the semiconductor device 300, resulting in the semiconductor device 300 illustrated in Fig. 5. Advantageously, the doped copper seed layer 50 essentially encapsulates the pure copper 30, resulting in improved electromigration resistance throughout the entire interconnect structure.

Thus, in accordance with the present invention, an interconnect is formed using essentially pure copper and doped copper. Advantageously, the resulting interconnect structure exhibits improved electromigration resistance in areas more susceptible to electromigration while maintaining low overall resistivity. A copper alloy seed layer 50 formed along the bottom and sidewalls of the interconnect opening further improves the electromigration resistance of the interconnect, thereby further improving the reliability of the semiconductor device. The present invention is also cost effective and can be easily integrated into conventional processing.

In the previous descriptions, numerous specific details are set forth, such as specific materials, structures,

chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the specific details set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention.

The dielectric and conductive layers used in manufacturing a semiconductor device in accordance with the present invention can be deposited by conventional deposition techniques. For example, metallization techniques, such as various types of chemical vapor deposition (CVD) processes, including low pressure chemical vapor deposition (LPCVD) and enhanced chemical vapor deposition (ECVD) can be employed.

The present invention is applicable in the manufacturing of semiconductor devices and particularly in semiconductor devices with design features of 0.25 microns and below, resulting in increased transistor and circuit speeds and improved reliability. The present invention is applicable to the formation of any of various types of semiconductor devices, and hence, details have not been set forth in order to avoid obscuring the thrust of the present invention. In practicing the present invention, conventional photolithographic and etching techniques are employed and, hence, the details of such techniques have not been set forth herein in detail.

Only the preferred embodiments of the invention and a few examples of its versatility are shown and described in the present disclosure. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of modifications within the scope of the inventive concept as expressed herein.

For example, the present invention has been described with the example of single level interconnects formed by created openings in a dielectric layer and filling the openings. The present invention is also applicable to other situations where interconnects are formed, such as dual damascene techniques which form a conductive via that contacts an upper trench section. In this scenario, the pure copper may be deposited in the conductive via and a portion of the conductive trench. The upper portion of the conductive trench may then be filled with doped copper.

WHAT IS CLAIMED IS:

1. A method of forming an interconnect in a semiconductor device (200), the method comprising:
forming an opening (24) in a dielectric layer (22);
depositing substantially pure copper (30) to fill a portion of the opening;
depositing doped copper (32) over the substantially pure copper (30) to fill the opening (24); and
planarizing the semiconductor device (200) so that the filled opening is substantially coplanar with an upper surface of the dielectric layer (22).

2. The method of claim 1, wherein the portion comprises about 40% to about 90% of the opening (24).

3. The method of claim 1, wherein the doped copper (32) contains about 0.3% to about 12% by weight of a dopant element.

4. A semiconductor device (200), comprising:
a semiconductor substrate (20);
a plurality of levels of dielectric layers and conductive layers formed on the semiconductor substrate (20); and
an interconnect formed in at least one of the dielectric layers, the interconnect electrically connecting at least two of the conductive layers or one of the conductive layers and an active region in the semiconductor substrate (20), the interconnect being characterized by:
a lower portion comprising substantially pure copper (30), and
an upper portion comprising doped copper (32).

5. The semiconductor device (200) of claim 4, wherein the lower portion comprises about 40% to about 90% of the interconnect.

6. The semiconductor device (300) of claim 4, further comprising:
a layer of doped copper (50) formed along the bottom (42) and sidewalls (40) of the interconnect, the doped copper (50) encapsulating the substantially pure copper (30) in the lower portion of the interconnect.

7. A method of manufacturing a semiconductor device (200), comprising:
forming a plurality of levels of dielectric layers and conductive layers on a semiconductor substrate (20);
forming an opening (24) in at least one of the dielectric layers;
depositing substantially pure copper (30) to fill a portion of the opening (24);
depositing doped copper (32) over the substantially pure copper (30) to fill the opening (24); and
planarizing the semiconductor device (200) so that the copper and doped copper filled opening is substantially coplanar with an upper surface of the dielectric layer.

8. The method of claim 7, wherein the doped copper contains about 0.3% to about 12% by weight of a dopant element.

9. The method of claim 8, wherein the dopant element comprises at least one of tin, zirconium, strontium, palladium, magnesium, chromium and tantalum.

10. The method of claim 7, comprising:

depositing the substantially pure copper (30) by electroplating, and

depositing the doped copper (32) by at least one of electroless plating and electroplating.

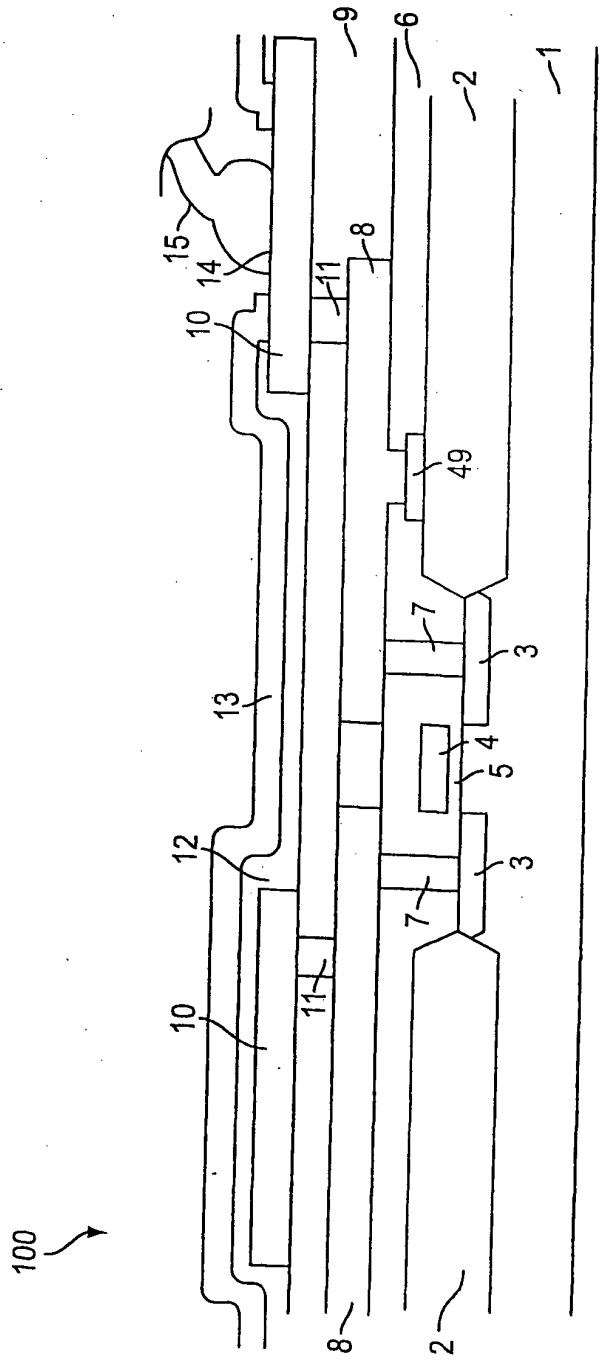

FIG. 1
(PRIOR ART)

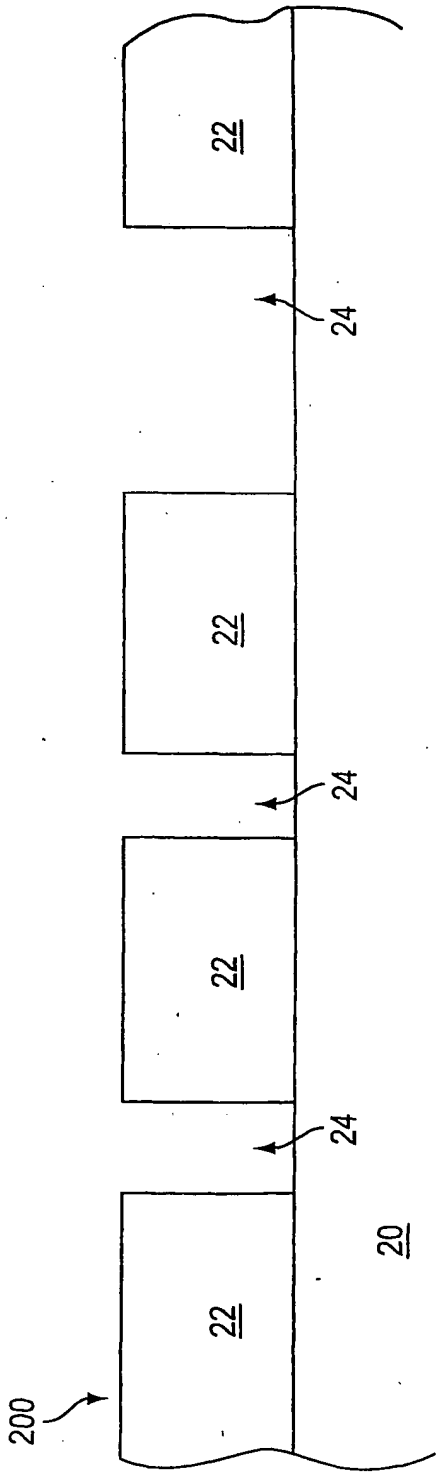

FIG. 2A

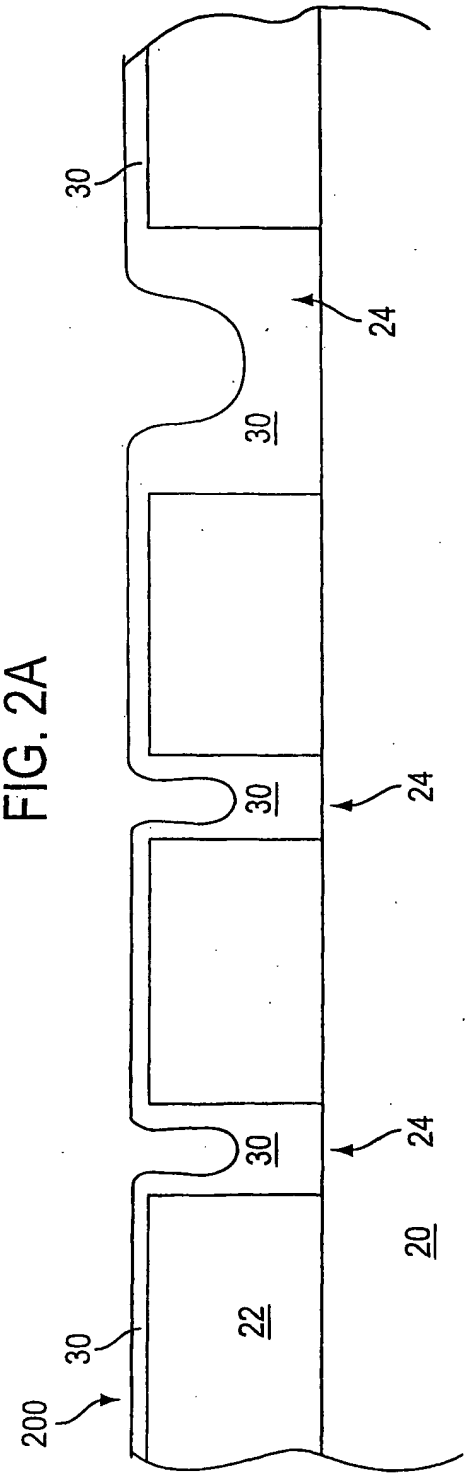

FIG. 2B

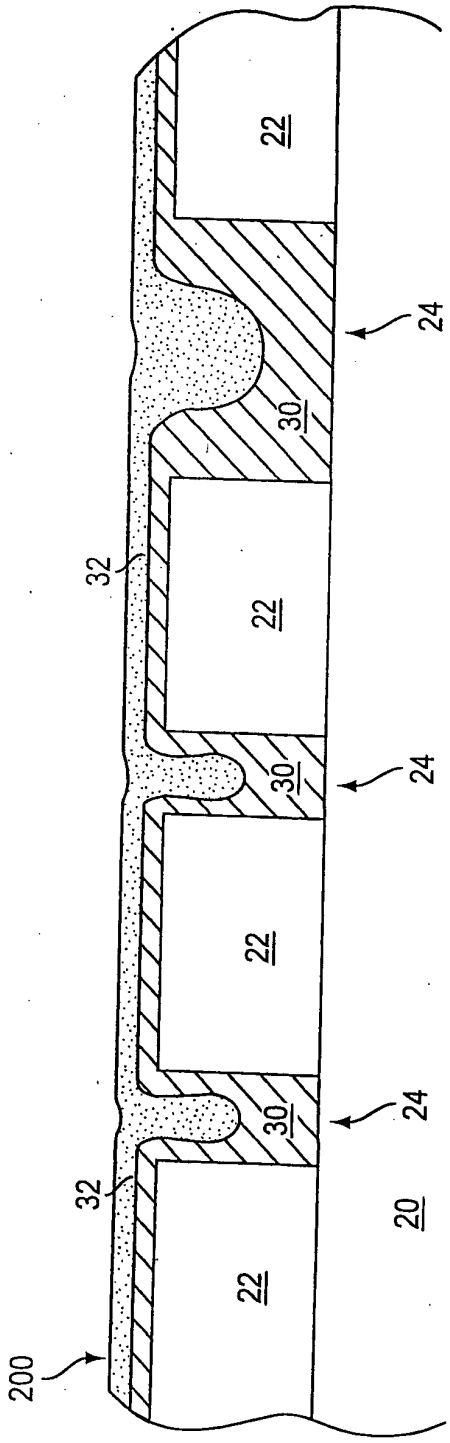

FIG. 3

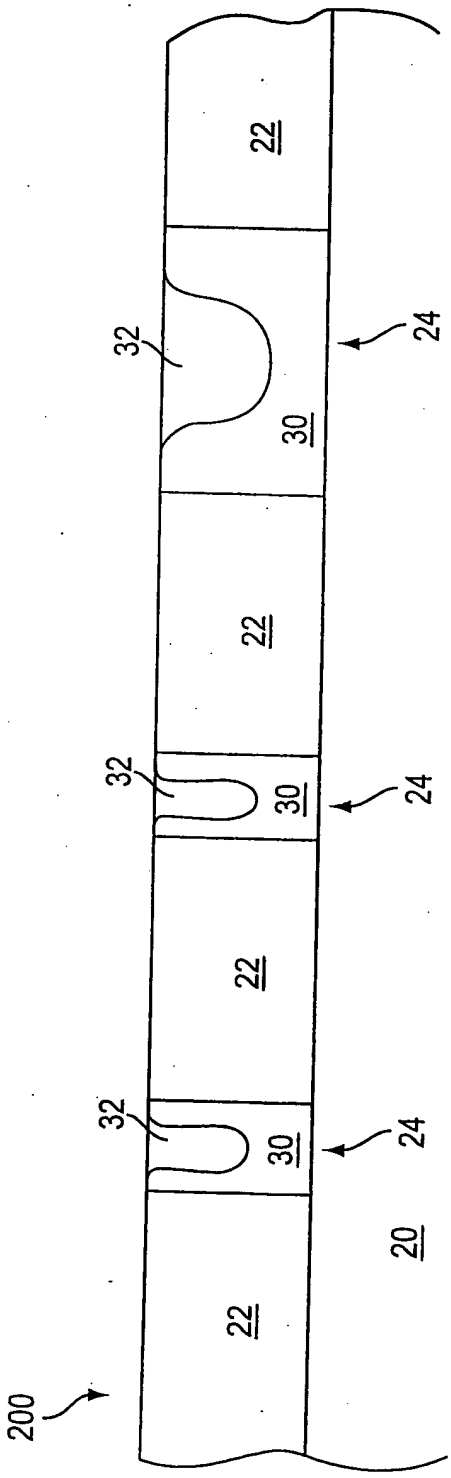

FIG. 4

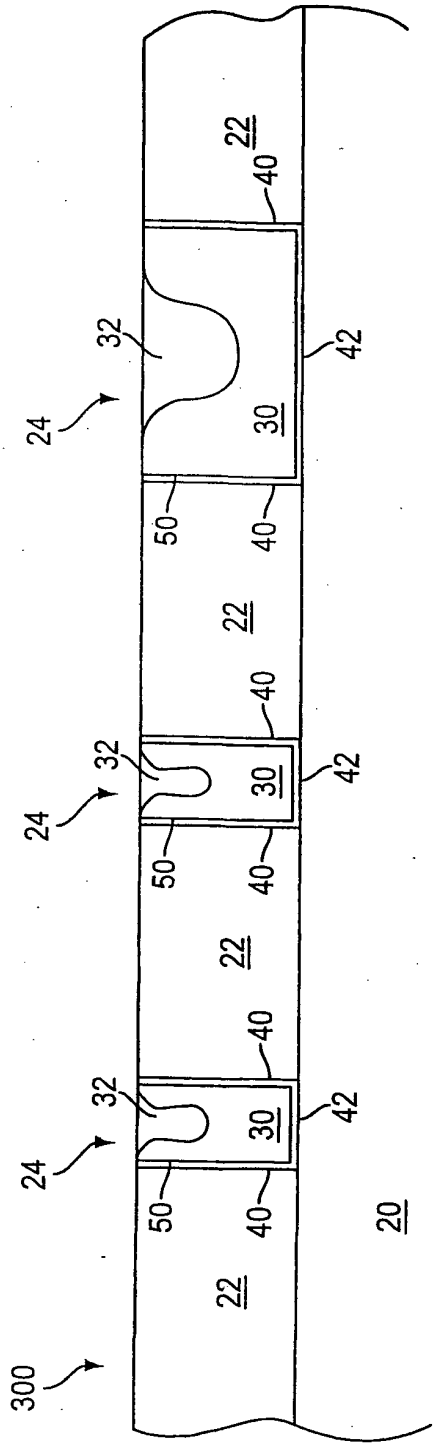

FIG. 5

INTERNATIONAL SEARCH REPORT

In ional Application No
PCT/US 01/10923

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
IBM-TDB, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 856 884 A (APPLIED MATERIALS INC) 5 August 1998 (1998-08-05) page 3, line 3-10 page 4, line 14-17	1,2,4-7
Y	page 5, line 6 -page 6, line 14 page 6, line 38-53; figures 1,2	3,8-10

Y	"CU(SN) ALLOYS FOR CHIP AND PACKAGE INTERCONNECTS" IBM TECHNICAL DISCLOSURE BULLETIN, IBM CORP. NEW YORK, US, vol. 37, no. 10, 1 October 1994 (1994-10-01), page 61 XP000475580 ISSN: 0018-8689 the whole document.	3,8-10

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
27 September 2001	08/10/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Boetticher, H

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INTERNATIONAL SEARCH REPORT

In onal Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 5 814 557 A (FIORDALICE ROBERT W ET AL) 29 September 1998 (1998-09-29) the whole document	1-10

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INTERNATIONAL SEARCH REPORT

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Ir ional Application No
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